The Math & CS Dept. and
Center for Cybercrime Studies

Presents

Security Analysis of Testability and Emerging Technologies

by

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Date: Wednesday, November 28, 2018
Time: community hour 1:40 -2:40 pm
Room: Graduate Lab, 6.67

Abstract: Globalization of the IC design flow gives rise to numerous security/trust threats. An adversary can launch attacks such as IP/IC piracy, reverse engineering, malicious circuit modification, referred as Hardware Trojans, and side-channel analysis. The speaker will discuss the security ramifications of the test infrastructure and the emerging computing technologies and paradigms. Also, she will explain the security vulnerabilities induced by advanced design for testability (DfT) techniques that improve the test quality of an IC by providing access to its internals. Next, she will shed light on timing-based side channel attacks on NEMS relay based designs and show the impact of input-dependent timing variation of NEMS-based cipher implementations on their side-channel security.